METHOD AND SYSTEM FOR IMPROVING ACCESS LATENCY OF MULTIPLE BANK DEVICES

ABSTRACT

The present invention is directed to a technique for improving access latency of multiple bank DRAMs. According to an embodiment of the present invention, address lines may be swapped to improve DRAM access latency and performance. According to another embodiment of the present invention, SDRAM performance may be improved by increasing the likelihood that cycles may be interleaved thereby reducing the overhead associated with opening and closing banks. The aspects of the present invention may be applied to multiple bank DRAM, such as SDRAM, DDR devices and/or other shared resource, in accordance with the present invention.